REMARKS

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Miller (U.S. Patent No. 6,622,103). This rejection repeats the rejection presented by the Office Action mailed March 7, 2005. This rejection is respectfully traversed as detailed to follow.

In response to Applicant's arguments filed June 9, 2005 to the previous Office Action, the present Office Action states Applicant's argument that the claimed isolation buffer has a control input "for selectively varying a delay caused by the variable delay isolation buffer in a signal traveling from the signal input to the signal output," in claim 1 to distinguish over Miller is not persuasive. The Office Action states that an intended use must present a structural difference, or if the prior art cited is capable of performing the intended use, it meets the claim limitation. The Office Action continues stating in Miller col. 7, line 67 discloses that the "Z signal delay" is calibrated requiring it be selectively varied. The Office Action further states that Miller in col. 6, lines 34-37 discloses use of a computer timing circuit 46 for timing of the Z, DRIVE and COMPARE signals rendering claim 1 anticipated.

In response, Applicant maintains the tristating buffer 40 receiving the Z signal, see Miller col. 6, line 28, is not capable of performing the intended use of the variable delay isolation buffer of claim 1. The tristate buffer 40 is tristated by the Z signal, so the tristate buffer 40 either enables an output signal with the Z signal in one state, or disables the output with the Z signal in another state. The tri-state buffer does not delay a signal,

as claimed. Delaying the Z signal only delays when the output of tristate buffer 40 disabled, and does not delay any buffer signal.

Applicant's claim 1 and specification call for a variable delay isolation buffer, configured like the buffer 51 of Fig. 12, and not a tri-state buffer. As shown in Fig. 12, the power supply voltage V_H and V_L are changed to control the delay through the buffer 51. The buffer circuitry of Fig. 12 can be used in the variable delay isolation buffer 110 of Fig. 11, or buffers 50_1 and 50_2 of Fig. 8. A tri-state buffer typically has an output gate that enables or disables the output signal, and does not vary any delay provided through the buffer as does the variable delay buffer of applicant's Fig. 12.

Delaying the Z signal in Miller using computer timing circuit 46 does not delay the buffer output as in claim 1, it only delays disabling of the tristate buffer 40. Thus, the tristate buffer 40 receiving the Z input does not perform the claimed function of delaying a signal from a buffer input to a buffer output as claimed in claim 1. Claim 1 is, thus, believed allowable as not anticipated under 35 U.S.C. § 102 by Miller.

Claim 24 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Miller in view of Kwon et al., (U.S. Patent No. 5,070,297). Claim 24 is believed allowable as non-obvious over Miller in view of Kwon et al., based at least on its dependency on claim 1.

Claims 4-6 and 11-13 stand objected to as being dependent upon a rejected base claim, but would otherwise be allowable if rewritten in independent form. Based on the above remarks with respect to claim 1 on which these claims dependant, Applicant believes that these claims are now allowable in dependent form.

Claims 2, 3 and 7-10 are indicated to be allowed.

In light of the above remarks, all of pending claims 1-13 and 24 are now believed to be in condition for allowance. Accordingly, reconsideration and allowance of these claims is respectfully requested.

No fee is believed due for this response. Should a fee be due, the Commissioner is authorized to charge the fee to Deposit Account No. 06-1325.

Respectfully submitted,

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